sampling the noise shaped signal at a predetermined sampling frequency and generating a sampled output signal with a lower transition rate with respect to the predetermined sampling frequency by a predetermined multiple;

feeding back the sampled output signal as the feedback signal; and

outputting the sampled output signal as an output signal.

29.(new) The method of digital amplification of claim 28, further comprising outputting the sampled output signal through an H-bridge controller.

30.(new) The method of digital amplification of claim 28, wherein the sampling includes suppressing sampling of the noise shaped signal for a set number of clock cycles of a sampling frequency clock.

31.(new) The method of digital amplification of claim 30, wherein the suppressing sampling includes detecting a transition in the sampled output signal.

32.(new) The method of digital amplification of claim 28, wherein the outputting includes outputting a multi-state output signal with at least three states.

33.(new) The method of digital amplification of claim 28, wherein the noise shaping includes integrating the summed output signal through a plurality of integrator stages.

34.(new) A method of digital amplification, comprising:

summing an input signal with a feedback signal and generating a summed output signal;

noise shaping the summed output signal and generating a noise shaped signal;

sampling the noised shaped signal and generating a sampled output signal;

feeding back the sampled output signal as the feedback signal; and

generating a multi-state output signal having at least three states using the sampled output signal.

35.(new) The method of digital amplification of claim 34, wherein a semiconductor H-bridge controller generates the multi-state output signal.

36.(new) The method of digital amplification of claim 35, wherein the sampling includes generating a sampled output signal having a lower transition rate with respect to a sampling frequency by a predetermined multiple.

37.(new) The method of digital amplification of claim 36, wherein the sampling includes suppressing sampling of the noise shaped signal for a set number of clock cycles of a sampling frequency clock.

38.(new) The method of digital amplification of claim 37, wherein the suppressing sampling includes detecting a transition in the output signal.

39.(new) The method of digital amplification of claim 38, wherein the noise shaping includes integrating the summed output signal through a plurality of integrator stages.

Claims 4 - 6, 11 - 27 remain unchanged by this Amendment and are included herein below for the Examiner's reference convenience.

4.(unchanged) A semiconductor H-bridge controller wherein its outputs consist of three states.

5.(unchanged) A semiconductor H-bridge controller of Claim 4 wherein the gating mechanism for each leg is independently controlled.

6.(unchanged) A digital amplifier comprising:

a modulation stage for signal shaping; and

a semiconductor H-bridge controller wherein its outputs consist of three states.

11.(unchanged) A digital amplifier comprising:

a modulation stage for signal shaping; and

a semiconductor H-bridge controller which generates a multi-state output.

12.(unchanged) The digital amplifier of claim 5, wherein the semiconductor H-bridge controller a multi-state output, includes at least three states.

13.(unchanged) The digital amplifier of claim 6, wherein the semiconductor H-bridge controller has two output terminals, and the output signal on each terminal is independently controlled.

14.(unchanged) A digital amplifier, comprising:

a summation circuit for summing an input signal with a feedback signal, and generating a summed output signal;

a noise shaping network with an input coupled to the output of the summation circuit and generating a noise shaped signal;

a sampling stage with an input connected to the output of the noise shaping network, and generating a sampled signal, the sampling stage having a predetermined sampling frequency, and generating an output signal with a lower transition rate with respect to the sampling frequency by a predetermined multiple;

a feedback loop providing the output of the sampling stage coupled directly to the summation circuit; and

an output stage with inputs connected to the output of the sampling stage and generating an output signal.

15. (unchanged) The digital amplifier of claim 14, wherein the output stage includes an H-bridge controller.

16. (unchanged) The digital amplifier of claim 14, wherein the sampling stage further comprises a logic circuit for suppressing sampling of the input signal for a set number of clock cycles of the sampling frequency clock.

17. (unchanged) The digital amplifier of claim 16, wherein the logic circuit further includes a transition detector for detecting a transition in the output signal.

18. (unchanged) The digital amplifier of claim 14, wherein the output signal of the sampling stage has a multi-state output, with at least three states.

19. (unchanged) The digital amplifier of claim 14, wherein the noise shaping network comprises a plurality of integrator stages.

20. (unchanged) A digital amplifier, comprising:

a summation circuit for summing an input signal with a feedback signal, and generating a summed output signal;

a noise shaping network with an input coupled to the output of the summation circuit and generating a noise shaped signal;

a sampling stage with an input connected to the output of the noise shaping network, and generating an output signal with a multi-state output, with an least three states;

a feedback loop providing the output of the sampling stage coupled directly to the summation circuit; and

an output stage with inputs connected to the output of the sampling stage and generating an output signal.

21. (unchanged) The digital amplifier of claim 14, wherein the output stage includes a semiconductor H-bridge controller.

22. (unchanged) The digital amplifier of claim 14, wherein the sampling circuit generates an output signal with a lower transition rate with respect to the sampling frequency by a predetermined multiple.

23. (unchanged) The digital amplifier of claim 14, wherein the sampling circuit further comprises a logic circuit for suppressing sampling of the input signal for a set number of clock cycles of the sampling frequency clock.

24. (unchanged) The digital amplifier of claim 17, wherein the logic circuit further comprises a transition detector for detecting a transition in the output signal.

25. (unchanged) The digital amplifier of claim 14, wherein the noise shaping network comprises a plurality of integrator stages.

26. (unchanged) A semiconductor H-bridge controller which generates a multi-state output, with at least three states.

27. (unchanged) The semiconductor H-bridge controller of claim 26, wherein the semiconductor H-bridge controller has two output terminals, and the output signal on each terminal is independently controlled.